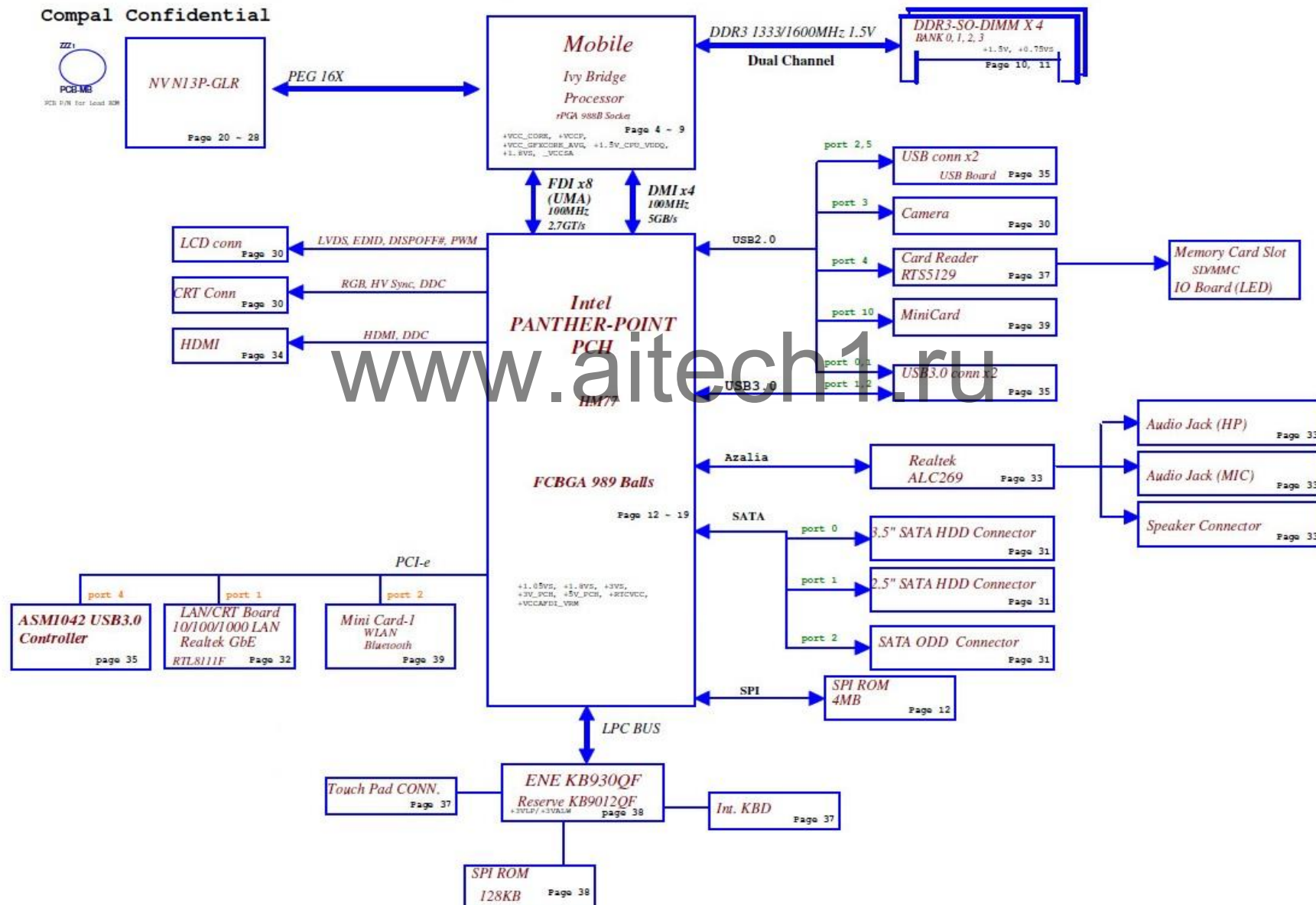
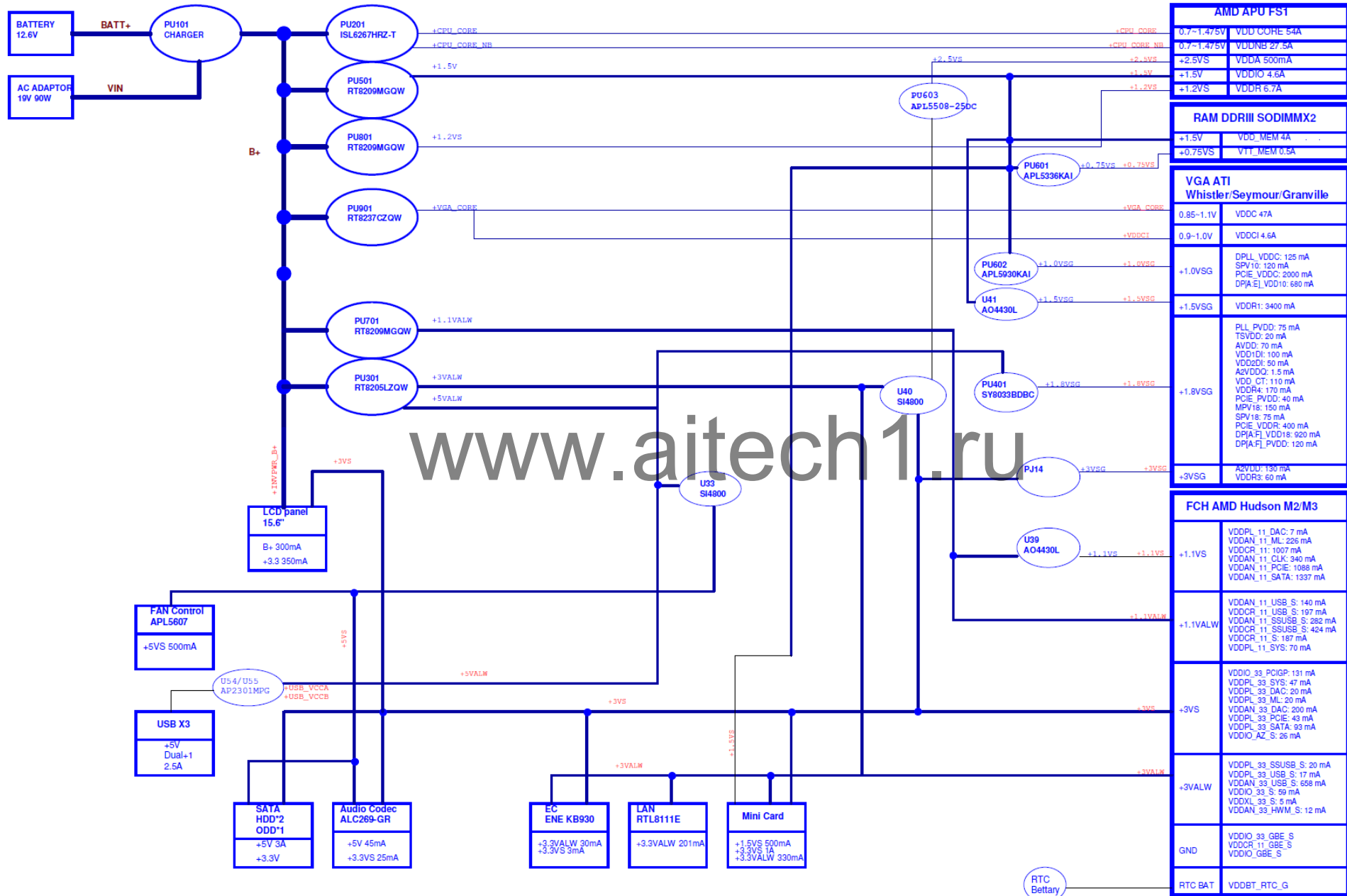


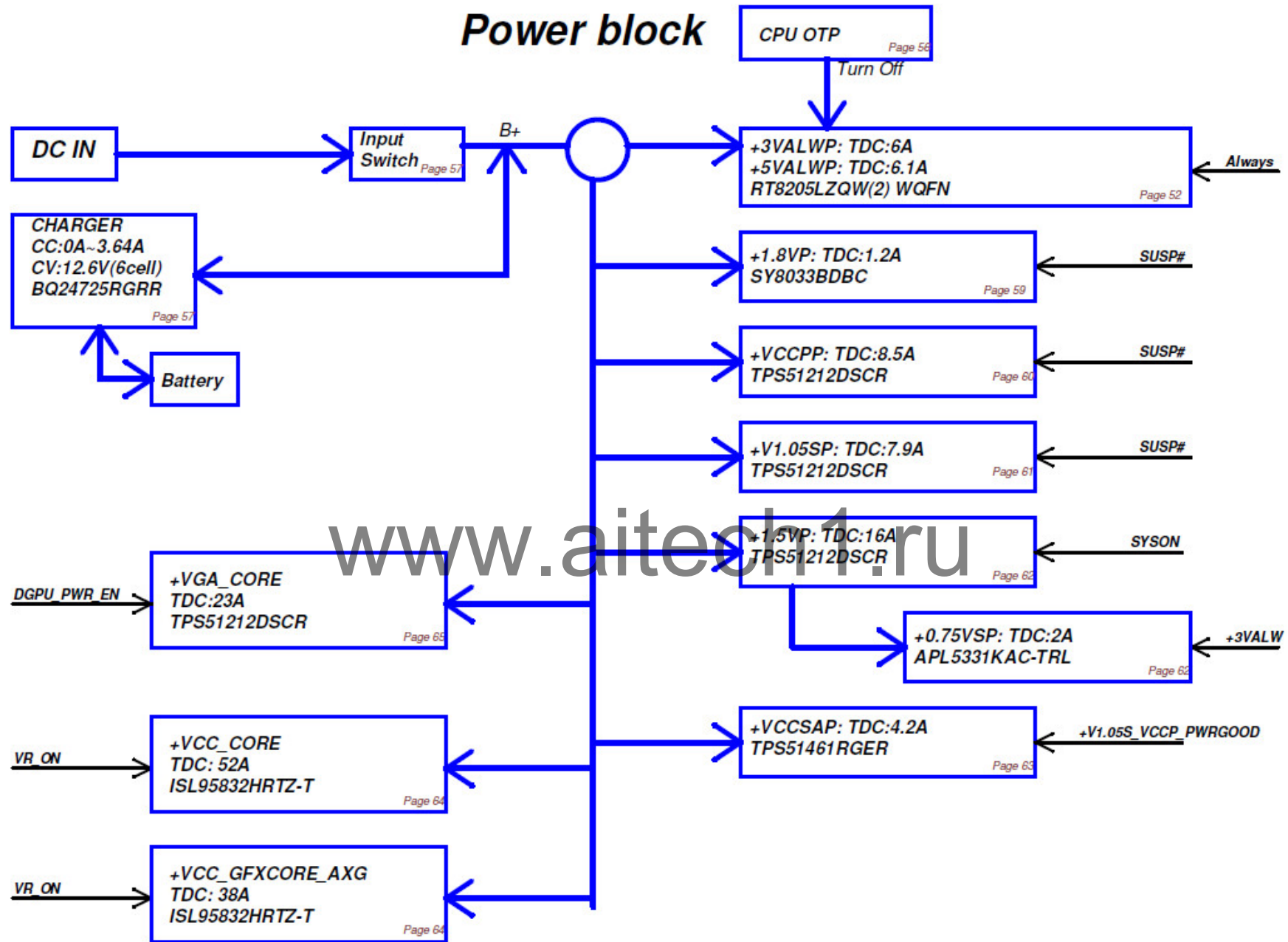
BLOCK DIAGRAM QCL90



POWER FLOW

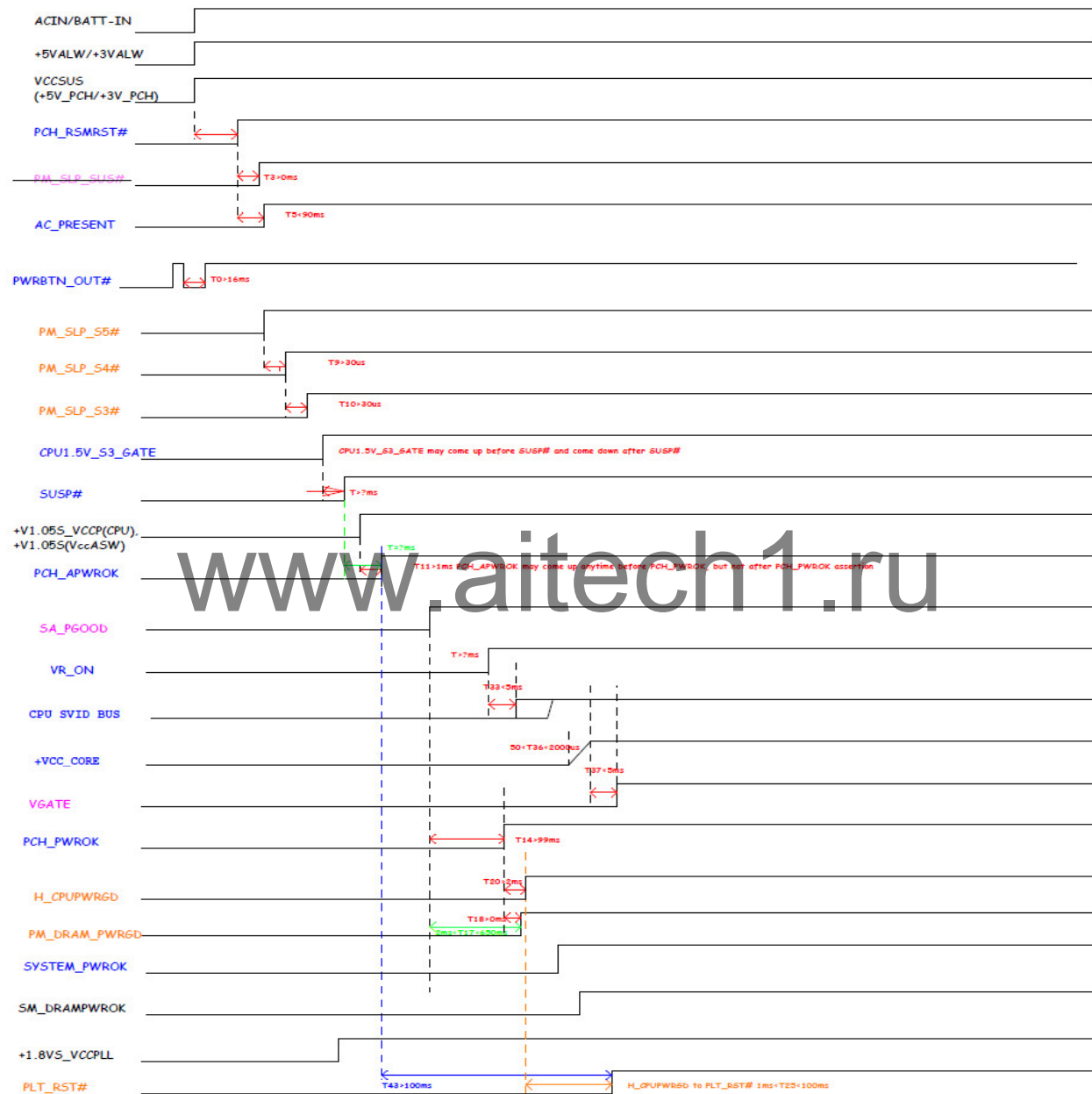


Power block



POWER ON SEQUENCE

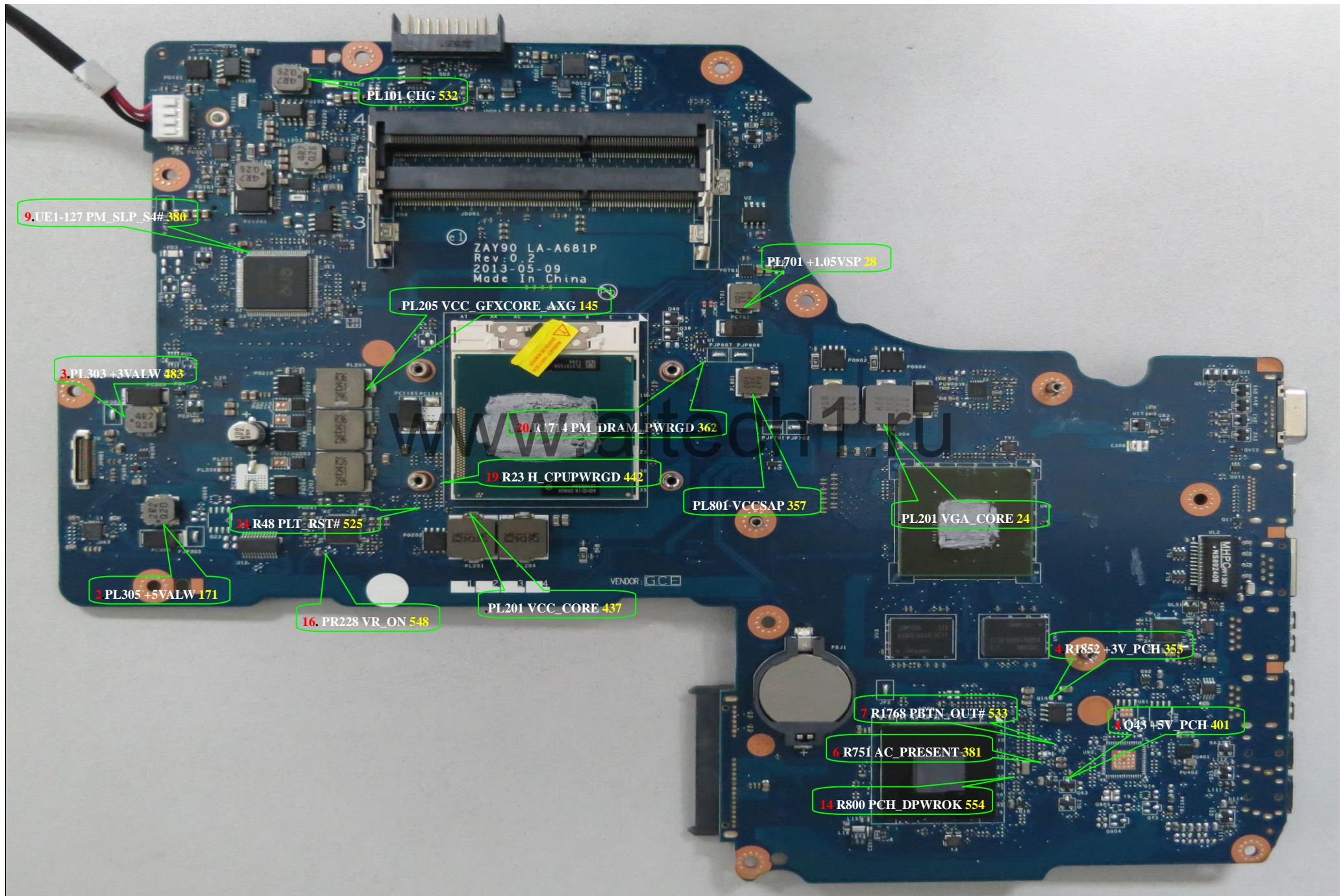
Timing Diagram for G3 or S4-S/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



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Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Signal Measure Point-Bottom



Signal Measure Point-Top

